# Amjad Hamed ENG2025 Coursework Report – Serial Multiplier

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Module: Digital Electronics

Title: Structural VHDL Design of a 4x4-bit Serial Multiplier

EDAPlayground Link: https://www.edaplayground.com/x/w3r3

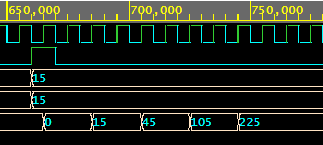
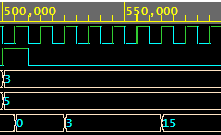
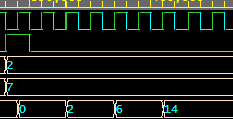
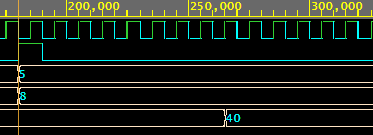
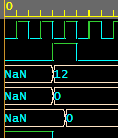
## Introduction: Design Process & Choices

In this design, a 4-bit serial multiplier is designed and implemented. The serial multiplier works by shifting the multiplicand and multiplier bit-by-bit while adding up the partial products at each step.

* Choice of Shift Registers: The shift registers are used to hold the multiplier and multiplicand (R and D). These registers allow the multiplier to shift its bits, enabling the bit-by-bit multiplication.
* 8-bit Adder: The adder is responsible for adding the partial product at each step. Event-based logic is used to control the shifts and additions.
* Shift Process: At each clock cycle, the least significant bit of the multiplier is ANDed with the multiplicand, and the result is added to the product register.

## Implementation Details

* The design uses RTL and structural techniques for the shift registers and adder components.
* Delay Consideration: The ripple-carry adder used in the serial multiplier introduces a delay due to the sequential carrying of bits across each adder. In this design, the adder's delay is proportional to the number of bits being added, and it increases the more bits. For a 4-bit serial multiplier, the delay is manageable, but for larger designs, this delay could significantly impact the speed. The delay in the adder is a trade-off for a simpler design, as more complex adders, such as carry-lookahead adders (CLA), could improve performance at the cost of added hardware complexity.
* The testbench applies a series of values in the range of 0 to 15 to test the functionality of the serial multiplier.
* Testbench Setup:
  + Inputs: Various combinations of A = 5, B = 3 and A = 15, B = 15 are tested to observe the correct functioning of the serial multiplication process.
  + Simulation Results: The serial multiplier operates correctly, shifting the values and adding partial products at each clock cycle.



## Conclusion

This design successfully implements the 4-bit serial multiplier, where the shift registers manage the shifting, and the adder accumulates the partial products. The testbench verified that the design produces the correct output for a wide range of test values. The simulation results confirmed that the design functions as intended.